



256K x 24 Static RAM Module

Features

- High-density 6-Megabit SRAM Module
- High-speed CMOS SRAMs
  - $t_{AA} = 10 \text{ ns}$
- Single 3.3V power supply
- Low active power(648 W at 10 ns)
- TTL-compatible Inputs and Outputs
- Available in standard 119-ball BGA

Functional Description

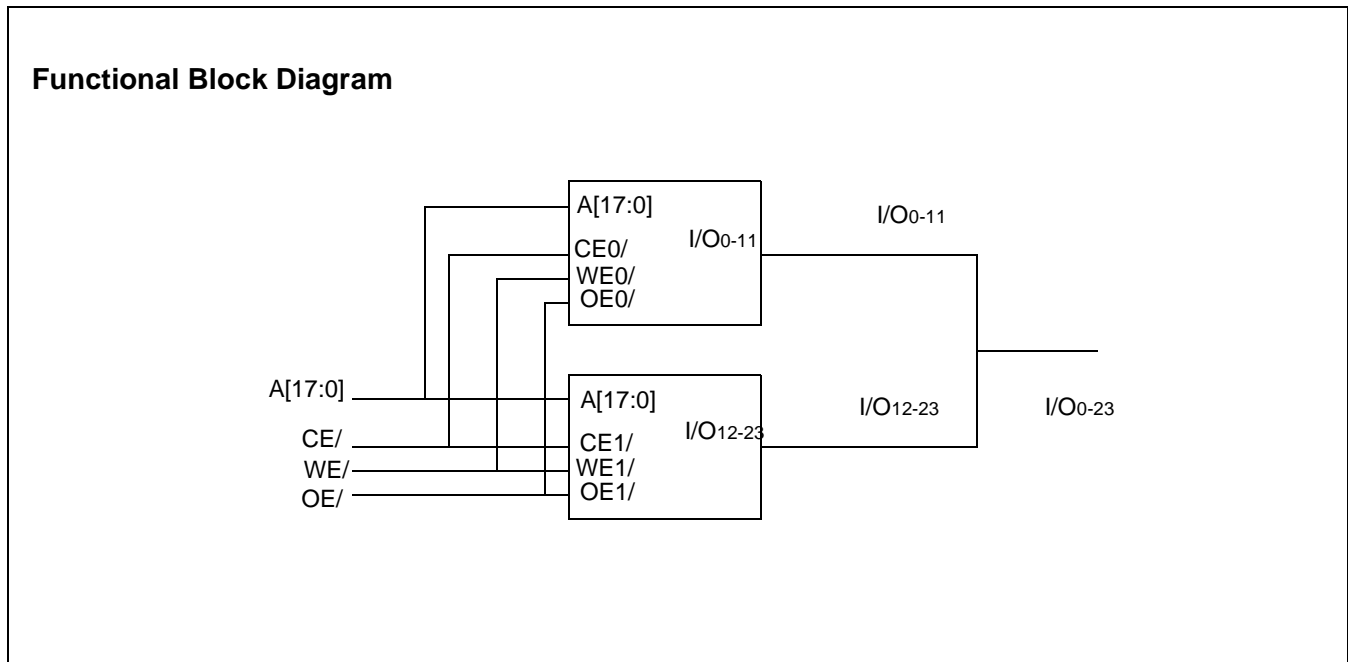
The CYM26KAH24AV33 is a 3.3V high-performance 6-Megabit static RAM organized as a 256K words by 24 bits. This module is constructed from two SRAM dies mounted on a multilayer laminate substrate combined to form a 24-bit SRAM.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data from I/O pins ( $I/O_0$  through  $I/O_{23}$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. Then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_{23}$ . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_{23}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), and the outputs are disabled ( $\overline{OE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CYM26KAH24AV33 is available in a standard 119 BGA.



Selection Guide

		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Commercial	180	170	mA
	Industrial	200	190	mA
Maximum Standby Current	Commercial	20	20	mA
	Industrial			

**Pin Configurations**
**119 BGA  
Top View**

	1	2	3	4	5	6	7
<b>A</b>	NC	A	A	A	A	A	NC
<b>B</b>	NC	A	A	$\overline{CE}$	A	A	NC
<b>C</b>	I/O12	NC	NC <sup>[1]</sup>	A	NC <sup>[1]</sup>	NC	I/O11
<b>D</b>	I/O13	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O10
<b>E</b>	I/O14	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	I/O9
<b>F</b>	I/O15	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O8
<b>G</b>	I/O16	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	I/O7
<b>H</b>	I/O17	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O6
<b>J</b>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>DD</sub>
<b>K</b>	I/O18	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O5
<b>L</b>	I/O19	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	I/O4
<b>M</b>	I/O20	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O3
<b>N</b>	I/O21	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	I/O2
<b>P</b>	I/O22	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O1
<b>R</b>	I/O23	NC	NC	NC	NC	NC	I/O0
<b>T</b>	NC	A	A	$\overline{WE}$	A	A	NC
<b>U</b>	NC	A	A	$\overline{OE}$	A	A	NC

**Note:**

1. Bumps 3C and 5C are actually NC's but they should be wired 3C to V<sub>CC</sub> and 5C to V<sub>SS</sub> to assure compatibility with future versions.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied.. -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> ..... -0.5V to 4.6V  
 DC Voltage Applied to Outputs in High-Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current..... > 200 mA

**Operating Range**

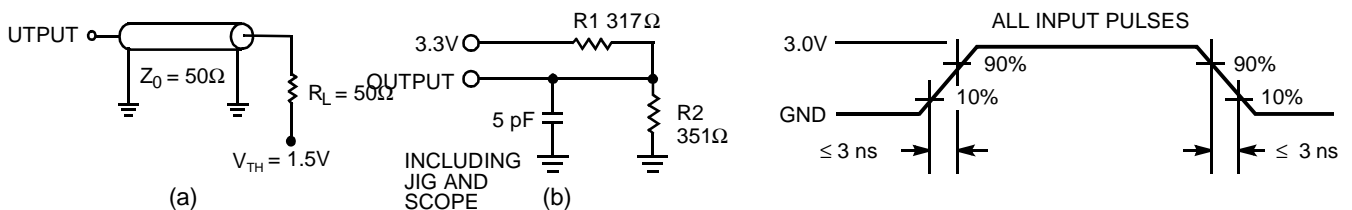
Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ±5%
Industrial	-40°C to +85°C	3.3V ±5%

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	-10		-12		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-2	+2	-2	+2	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-2	+2	-2	+2	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max. f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial	180		170	mA
			Industrial	200		190	mA
I <sub>SB1</sub>	Automatic CE Power-down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		80		80	mA
I <sub>SB2</sub>	Automatic CE Power-down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Commercial/Industrial	20		20	mA

**Capacitance<sup>[2]</sup>**

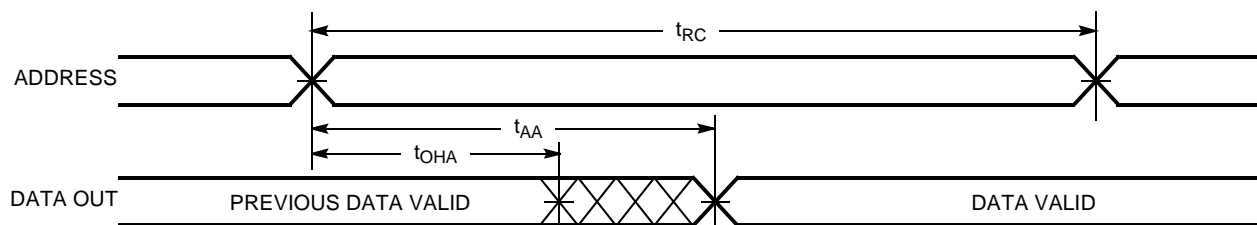
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	10	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**AC Test Loads and Waveforms**

**Note:**

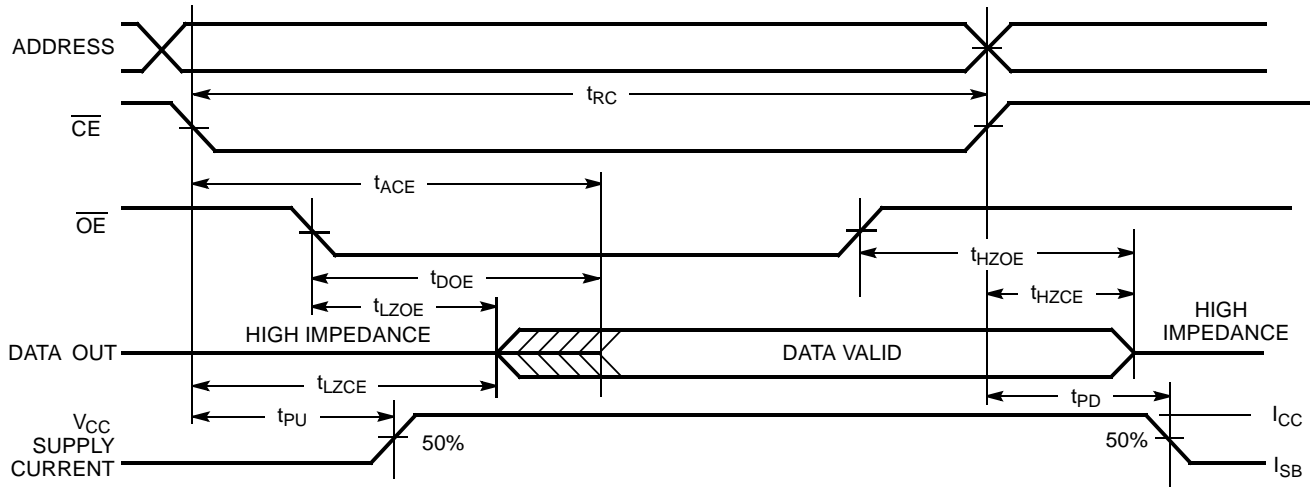
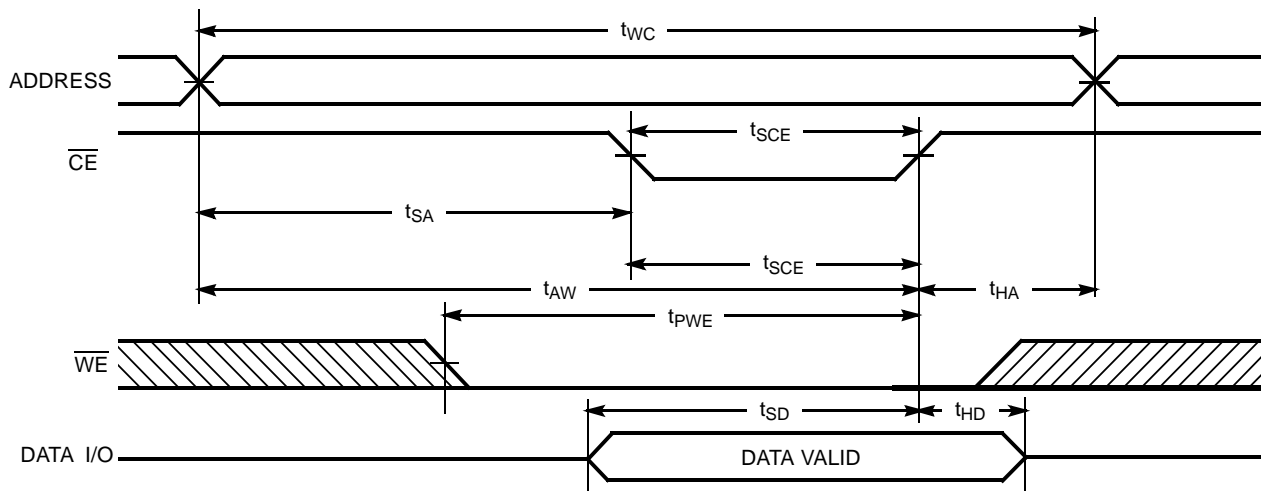
2. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.

**AC Switching Characteristics<sup>[3]</sup> Over the Operating Range**

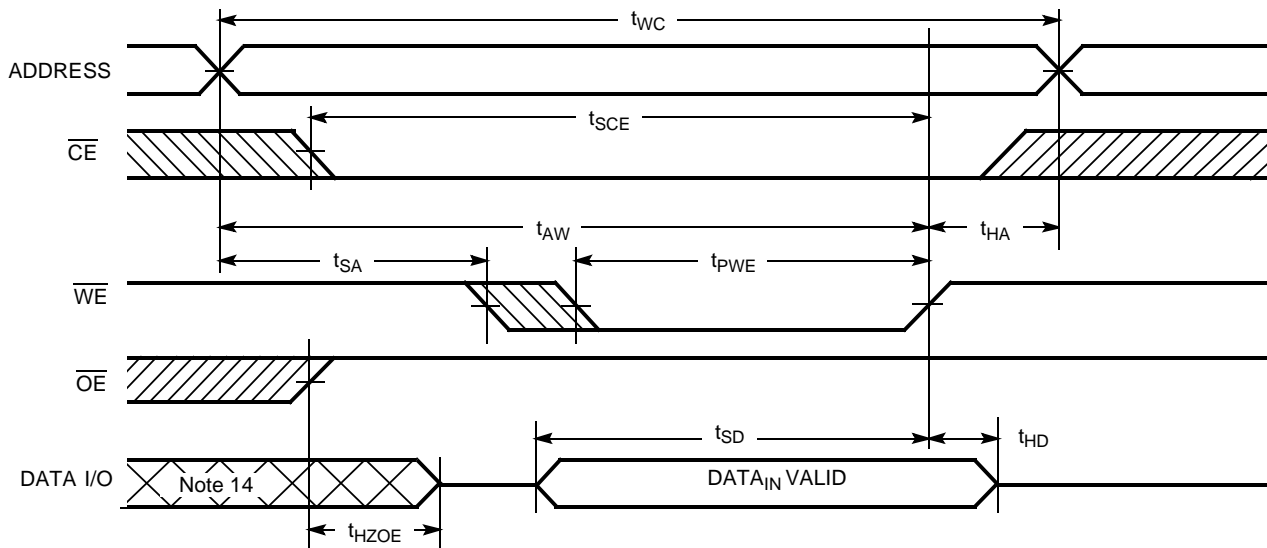
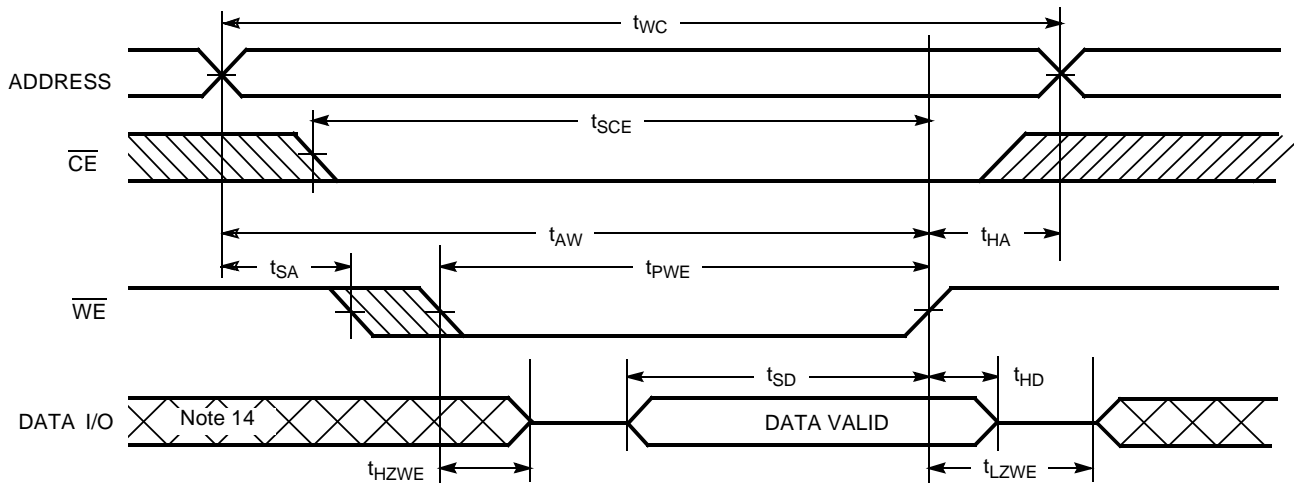
Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	10		12		ns
$t_{AA}$	Address to Data Valid		10		12	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	CE active to Data Valid		10		12	ns
$t_{DOE}$	OE LOW to Data Valid		5		6	ns
$t_{LZOE}$	OE LOW to Low Z	0		0		ns
$t_{HZOE}$	OE HIGH to High Z <sup>[4, 5]</sup>		5		6	ns
$t_{LZCE}$	CE active to Low Z <sup>[5]</sup>	3		3		ns
$t_{HZCE}$	CE inactive to High Z <sup>[4, 5]</sup>		5		6	ns
$t_{PU}$	CE active to Power-Up	0		0		ns
$t_{PD}$	CE inactive to Power-Down		10		12	ns
<b>Write Cycle<sup>[6, 7]</sup></b>						
$t_{WC}$	Write Cycle Time	10		12		ns
$t_{SCE}$	CE active to Write End	7		8		ns
$t_{AW}$	Address Set-Up to Write End	7		8		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	WE Pulse Width	7		8		ns
$t_{SD}$	Data Set-Up to Write End	5		6		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	WE HIGH to Low Z <sup>[5]</sup>	3		3		ns
$t_{HZWE}$	WE LOW to High Z <sup>[4, 5]</sup>		4		5	ns

**Switching Waveforms**
**Read Cycle No. 1<sup>[8, 9]</sup>**

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$ .
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- Device is continuously selected. OE, CE =  $V_{IL}$ .

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>**

**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[12, 13]</sup>**

**Notes:**

10.  $\overline{WE}$  is HIGH for read cycle.
11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
12. Data I/O is high impedance if  $OE = V_{IH}$ .
13. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)**

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**

**Ordering Information**

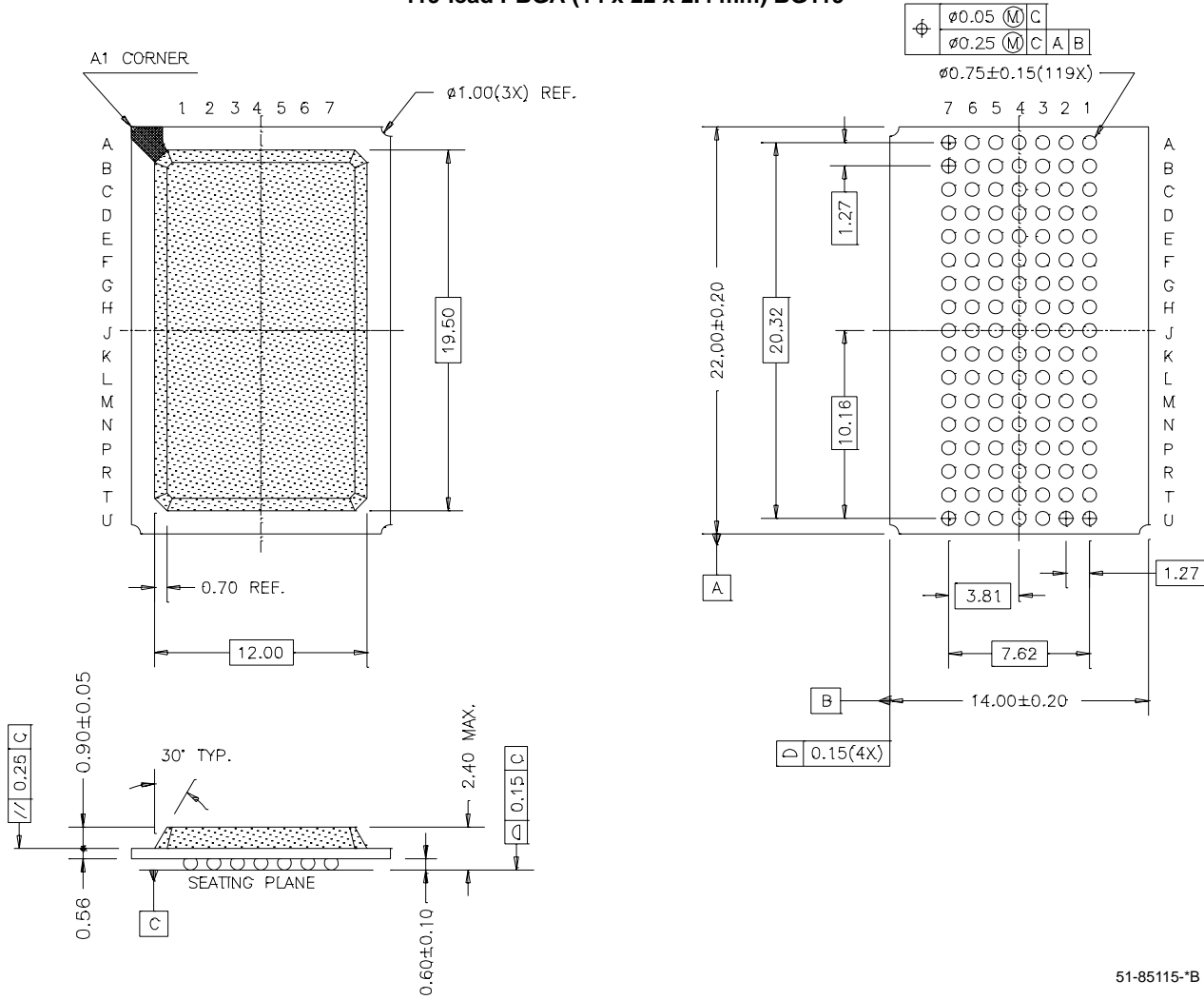
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CYM26KAH24AV33-10BGC	BG119	119-Ball BGA	Commercial
10	CYM26KAH24AV33-10BGI	BG119	119-Ball BGA	Industrial
12	CYM26KAH24AV33-12BGC	BG119	119-Ball BGA	Commercial
12	CYM26KAH24AV33-12BGI	BG119	119-Ball BGA	Industrial

**Note:**

14. During this period the I/Os are in the output state and input signals should not be applied.

Package Diagram

119-lead PBGA (14 x 22 x 2.4 mm) BG119



51-85115-B

All product and company names mentioned in this document are the trademarks of their respective holders.



**Document History Page**

<b>Document Title: CYM26KAH24AV33 256K x 24 Static RAM Module</b> <b>Document Number: 38-05324</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	123014	01/22/03	CS	New Data Sheet